REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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Original date of drawing
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12-10-12

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TITLE

MICROCIRCUIT, LINEAR, LOW VOLTAGE, 1.15 V TO 5.5 V, 4-CHANNEL, BIDIRECTIONAL LOGIC LEVEL TRANSLATOR, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12631

REV

PAGE 1 **OF** 11

AMSC N/A

5962-V009-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low voltage, 1.15 V to 5.5 V, 4-channel bidirectional logic level translator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12631	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG3304-EP	Low voltage, 1.15 V to 5.5 V, 4-channel bidirectional logic level translator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MO-153-AB-1	Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{CCA} to GND	-0.3 V to +7.0 V
V_{CCY} to GND	V_{CCA} to +7.0 V
Digital inputs (A)	-0.3 V to (V_{CCA} + 0.3 V)
Digital inputs (Y)	-0.3 V to (V_{CCY} + 0.3 V)
EN to GND	-0.3 V to +7.0 V
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
θ_{JA} Thermal impedance (4 layer board) , Case outline X	112.6°C/W
Lead temperature, soldering:	
Vapor phase (60 sec)	215°C
Infrared (15 sec)	220°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
LOGIC INPUTS/OUTPUTS						
A side						
Input high voltage 4/	V_{IHA}	V_{CCA} = 1.2 V + 0.1 V/-0.05 V	V_{CCA} x 0.88			V
		V_{CCA} = 1.8 V ±0.15 V	V_{CCA} x 0.72			
		V_{CCA} = 2.5 V ±0.2 V	1.7			
		V_{CCA} = 3.3 V ±0.3 V	2.2			
		V_{CCA} = 5 V ±0.5 V	V_{CCA} x 0.7			
Input low voltage 4/	V_{ILA}	V_{CCA} = 1.2 V + 0.1 V/-0.05 V			V_{CCA} x 0.35	
		V_{CCA} = 1.8 V ±0.15 V			V_{CCA} x 0.35	
		V_{CCA} = 2.5 V ±0.2 V			0.7	
		V_{CCA} = 3.3 V ±0.3 V			0.8	
		V_{CCA} = 5 V ±0.5 V			V_{CCA} x 0.30	
Output high voltage	V_{OHA}	V_Y = V_{CCY}, I_{OH} = 20 µA	V_{CCA} – 0.4			
Output low voltage	V_{OLA}	V_Y = 0 V, I_{OL} = 20 µA			0.4	
Capacitance 4/	C_A	f = 1 MHz, EN = 0		9		pF
Leakage current	$I_{LA, HI-Z}$	V_A = 0 V/V_{CCA}, EN = 0			±1	µA
Y side						
Input high voltage 4/	V_{IHY}	V_{CCY} = 1.8 V ±0.15 V	V_{CCY} x 0.67			V
		V_{CCY} = 2.5 V ±0.2 V	1.7			
		V_{CCY} = 3.3 V ±0.3 V	2			
		V_{CCY} = 5 V ±0.5 V	V_{CCY} x 0.7			
Input low voltage 4/	V_{ILY}	V_{CCY} = 1.8 V ±0.15 V			V_{CCY} x 0.35	
		V_{CCY} = 2.5 V ±0.2 V			0.7	
		V_{CCY} = 3.3 V ±0.3 V			0.8	
		V_{CCY} = 5 V ±0.5 V			V_{CCY} x 0.25	
Output high voltage	V_{OHY}	V_A = V_{CCA}, I_{OH} = 20 µA	V_{CCY} - 0.4			
Output low voltage	V_{OLY}	V_A = 0 V, I_{OL} = 20 µA			0.4	
Capacitance 3/	C_Y	f = 1 MHz, EN = 0		6		pF
Leakage current	$I_{LY, HI-Z}$	V_Y = 0 V/V_{CCY}, EN = 0			±1	µA
Enable (EN)						
Input high voltage 4/	V_{IHA}	V_{CCA} = 1.2 V + 0.1 V/-0.05 V	V_{CCA} x 0.88			
		V_{CCA} = 1.8 V ±0.15 V	V_{CCA} x 0.72			
		V_{CCA} = 2.5 V ±0.2 V	1.7			
		V_{CCA} = 3.3 V ±0.3 V	2.2			
		V_{CCA} = 5 V ±0.5 V	V_{CCA} x 0.7			
Input low voltage 4/	V_{ILA}	V_{CCA} = 1.2 V + 0.1 V/-0.05 V			V_{CCA} x 0.35	
		V_{CCA} = 1.8 V ±0.15 V			V_{CCA} x 0.35	
		V_{CCA} = 2.5 V ±0.2 V			0.7	
		V_{CCA} = 3.3 V ±0.3 V			0.8	
		V_{CCA} = 5 V ±0.5 V			V_{CCA} x 0.30	
Leakage current	I_{LEN}				±1	µA
Capacitance 3/	C_{EN}			3		pF
Enable time 4/	t_{EN}	R_S = R_T = 50 Ω, V_A = 0 V/V_{CCA} (A→Y), V_Y = 0 V/V_{CCY} (Y→A)		1	1.8	µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
SWITCHING CHARACTERISTICS 4/						
3.3 V ± 0.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 5 V ± 0.5 V						
A → Y level translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation delay	$t_{P, A\rightarrow Y}$			6	15	ns
Rise time	$t_{R, A\rightarrow Y}$			2	5	ns
Fall time	$t_{F, A\rightarrow Y}$			2	5	ns
Maximum data rate	$D_{MAX, A\rightarrow Y}$			50		Mbps
Channel to channel skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part to part skew	$t_{PSKEW, A\rightarrow Y}$			3		ns
Y → A level translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation delay	$t_{P, Y\rightarrow A}$			4	10	ns
Rise time	$t_{R, Y\rightarrow A}$			1	5	ns
Fall time	$t_{F, Y\rightarrow A}$			3	10	ns
Maximum data rate	$D_{MAX, Y\rightarrow A}$			50		Mbps
Channel to channel skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part to part skew	$t_{PSKEW, Y\rightarrow A}$			2		ns
1.8 V ± 0.15 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A → Y translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation delay	$t_{P, A\rightarrow Y}$			8	15	ns
Rise time	$t_{R, A\rightarrow Y}$			2	8	ns
Fall time	$t_{F, A\rightarrow Y}$			2	8	ns
Maximum data rate	$D_{MAX, A\rightarrow Y}$			50		Mbps
Channel to channel skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part to part skew	$t_{PSKEW, A\rightarrow Y}$			4		ns
Y → A translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation delay	$t_{P, Y\rightarrow A}$			5	12	ns
Rise time	$t_{R, Y\rightarrow A}$			2	5	ns
Fall time	$t_{F, Y\rightarrow A}$			2	5	ns
Maximum data rate	$D_{MAX, Y\rightarrow A}$			50		Mbps
Channel to channel skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part to part skew	$t_{PSKEW, Y\rightarrow A}$			3		ns
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A → Y translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation delay	$t_{P, A\rightarrow Y}$			9	27	ns
Rise time	$t_{R, A\rightarrow Y}$			3	8	ns
Fall time	$t_{F, A\rightarrow Y}$			2	8	ns
Maximum data rate	$D_{MAX, A\rightarrow Y}$			40		Mbps
Channel to channel skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part to part skew	$t_{PSKEW, A\rightarrow Y}$			10		ns
Y → A translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation delay	$t_{P, Y\rightarrow A}$			5	13	ns
Rise time	$t_{R, Y\rightarrow A}$			2	6	ns
Fall time	$t_{F, Y\rightarrow A}$			2	6	ns
Maximum data rate	$D_{MAX, Y\rightarrow A}$			40		Mbps
Channel to channel skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part to part skew	$t_{PSKEW, Y\rightarrow A}$			4		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ 3/	Max	
SWITCHING CHARACTERISTICS – Continued. 4/						
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 1.8 V ± 0.3 V						
A → Y translation		R_S = R_T = 50 Ω, C_L = 50 pF				
Propagation delay	$t_{P, A→Y}$			12	35	ns
Rise time	$t_{R, A→Y}$			7	18	ns
Fall time	$t_{F, A→Y}$			3	8	ns
Maximum data rate	$D_{MAX, A→Y}$			25		Mbps
Channel to channel skew	$t_{SKEW, A→Y}$			2		ns
Part to part skew	$t_{PSKEW, A→Y}$			15		ns
Y → A translation		R_S = R_T = 50 Ω, C_L = 15 pF				
Propagation delay	$t_{P, Y→A}$			14	40	ns
Rise time	$t_{R, Y→A}$			5	24	ns
Fall time	$t_{F, Y→A}$			2.5	10	ns
Maximum data rate	$D_{MAX, Y→A}$			25		Mbps
Channel to channel skew	$t_{SKEW, Y→A}$			3		ns
Part to part skew	$t_{PSKEW, Y→A}$			23.5		ns
2.5 V ± 0.2 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A → Y translation		R_S = R_T = 50 Ω, C_L = 50 pF				
Propagation delay	$t_{P, A→Y}$			7	15	ns
Rise time	$t_{R, A→Y}$			2.5	6	ns
Fall time	$t_{F, A→Y}$			2	8	ns
Maximum data rate	$D_{MAX, A→Y}$			60		Mbps
Channel to channel skew	$t_{SKEW, A→Y}$			1.5		ns
Part to part skew	$t_{PSKEW, A→Y}$			4		ns
Y → A translation		R_S = R_T = 50 Ω, C_L = 15 pF				
Propagation delay	$t_{P, Y→A}$			5	12	ns
Rise time	$t_{R, Y→A}$			1	6	ns
Fall time	$t_{F, Y→A}$			3	8	ns
Maximum data rate	$D_{MAX, Y→A}$			60		Mbps
Channel to channel skew	$t_{SKEW, Y→A}$			2		ns
Part to part skew	$t_{PSKEW, Y→A}$			3		ns
POWER REQUIREMENTS						
Power supply voltages	V_{CCA}	V_{CCA} < V_{CCY}	1.15		5.5	V
	V_{CCY}		1.65		5.5	
Quiescent power supply current	I_{CCA}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.17	5	µA
	I_{CCY}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.27	5	
Three state mode power supply current	$I_{HI-Z, A}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.1	5	µA
	$I_{HI-Z, Y}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.1	5	

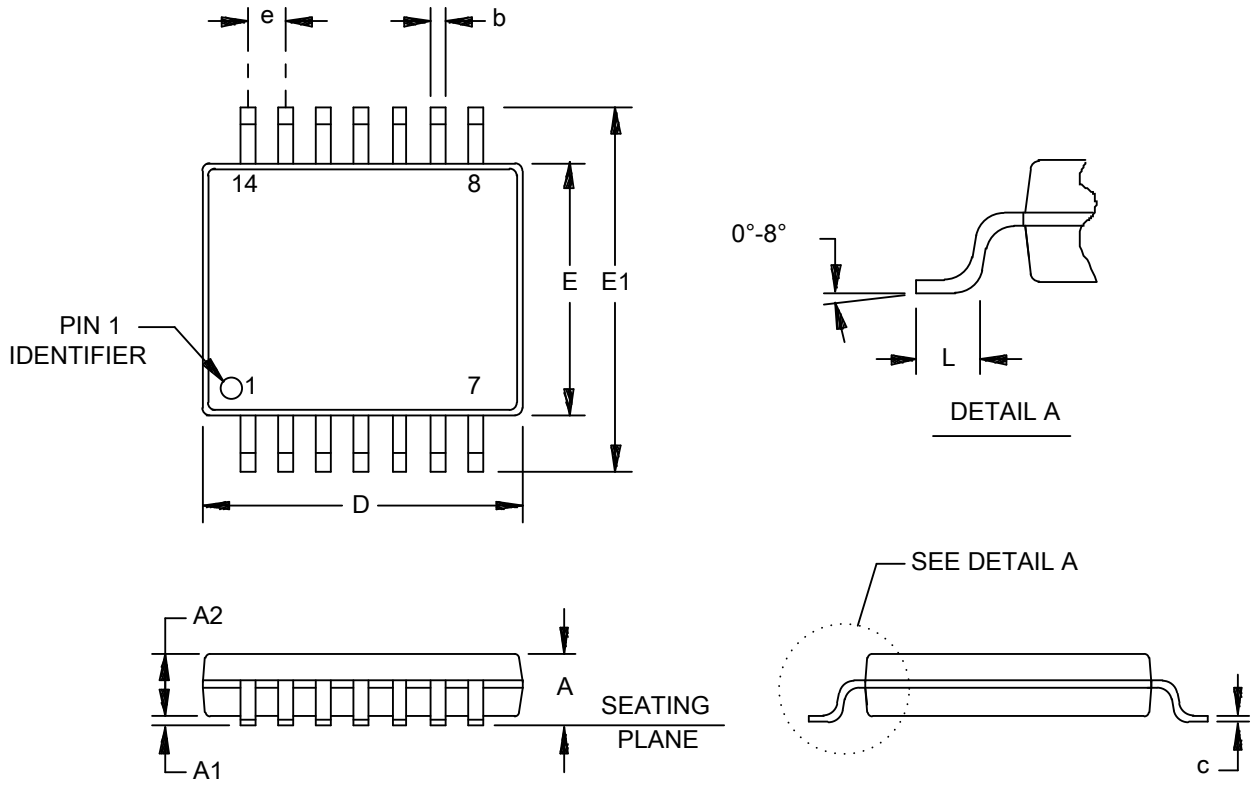
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ 1.65 V ≤ V_{CCY} ≤ 5.5 V, 1.15 V ≤ V_{CCA} ≤ V_{CCY}, GND = 0 V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified.

3/ T_A = 25°C for typical values.

4/ Guaranteed by design, not subject to production tested.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D	4.90	5.10
A1	0.05	0.15	E	4.30	4.50
A2	0.80	1.05	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AB-1.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CCA}	14	V_{CCY}
2	A1	13	Y1
3	A2	12	Y2
4	A3	11	Y3
5	A4	10	Y4
6	NC	9	NC
7	GND	8	EN

FIGURE 2. Terminal connections.

Terminal		Description
Number	Mnemonic	
1	V_{CCA}	Power supply voltage input for A1 to A4 I/O pins (1.15 V ≤ V_{CCA} ≤ V_{CCY})
2	A1	Input/Output A1. Reference to V_{CCA}
3	A2	Input/Output A2. Reference to V_{CCA}
4	A3	Input/Output A3. Reference to V_{CCA}
5	A4	Input/Output A4. Reference to V_{CCA}
6	NC	No Connect
7	GND	Ground
8	EN	Active high enable input
9	NC	No Connect
10	Y4	Input/Output Y4. Reference to V_{CCY}
11	Y3	Input/Output Y3. Reference to V_{CCY}
12	Y2	Input/Output Y2. Reference to V_{CCY}
13	Y1	Input/Output Y1. Reference to V_{CCY}
14	V_{CCY}	Power supply voltage input for Y1 to Y4 I/O pins (1.65 V ≤ V_{CC} ≤ 5.5 V)

FIGURE 3. Terminal function.

EN	Y I/O Pins	A I/O Pins
0	Hi-Z 1/	Hi-Z 1/
1	Normal operation 2/	Normal operation 2/

1. High impedance state.
2. In normal operation, the device performs level translation.

FIGURE 4. Truth table

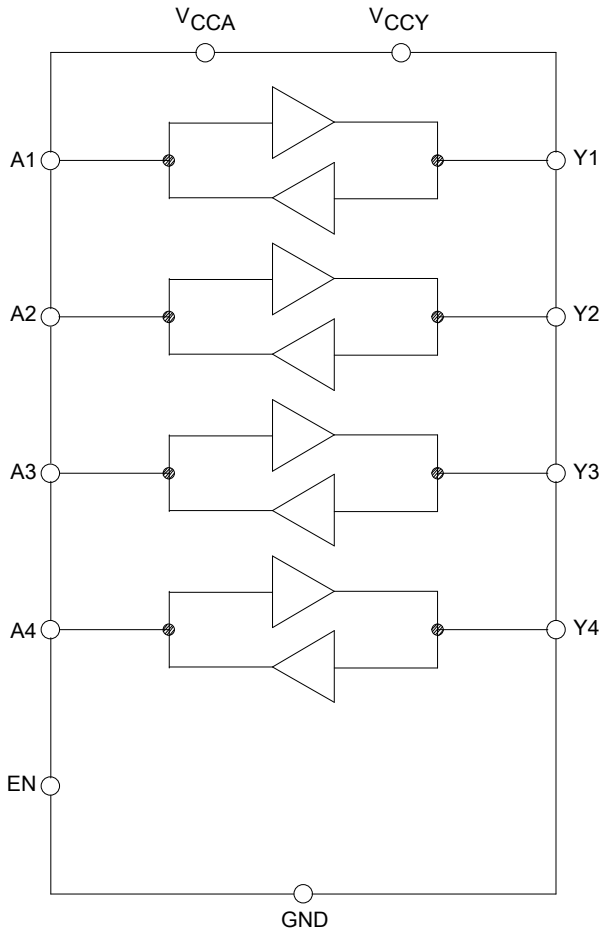


FIGURE 5. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12631-01XB	24355	ADG3304SRU-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106